

PHU HA TOAN

IC DESIGN INTERN



CONTACT

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EDUCATION

○ Ho Chi Minh City University of Technology (HCMUT), VNU-HCM

B.Eng. in Integrated Circuit Design

Expected Graduation: 09/27

GPA: 3.2

TECHNICAL SKILLS

- Cadence Virtuoso, Cadence Genus, LTspice
- Basic Synopsys tools, basic SystemVerilog
- Digital/analog circuits, CMOS fundamentals
- Technical documentation, Problem-solving, Teamwork

ADDITIONAL EXPOSURE

- RISC-V single-cycle and pipelined architecture
- Feedback amplifier design
- RTL design flow
- Basic analog and VLSI design laboratories

LANGUAGES

- Vietnamese
- English

CAREER OBJECTIVE

Third-year undergraduate student majoring in Integrated Circuit Design at Ho Chi Minh City University of Technology (HCMUT), VNU-HCM, seeking an internship in IC design and semiconductor engineering. Interested in digital and analog circuit design, CMOS fundamentals, and EDA-based circuit simulation.

ACADEMIC PROJECTS

○ 8×8 REGISTER BANK DESIGN USING D FLIP-FLOPS

Apr 2026 – May 2026

- Designing an 8×8 register bank using D flip-flops, decoder logic, and clock-gating techniques to reduce dynamic power consumption.
- Planning to use Cadence Genus for synthesis and report generation, including timing, area, and power analysis.
- Implementing schematic-level design and simulation in Cadence Virtuoso to study circuit behavior and design trade-offs.

○ LOW-POWER SENSE AMPLIFIER FOR SRAM

Feb 2026 – May 2026

- Designing and studying two SRAM sense amplifier topologies, including a baseline design and an enhanced topology for improved low-VDD operation.
- Evaluating offset tolerance, sensing delay, and power consumption, with Monte Carlo analysis for mismatch and offset behavior.
- Analyzing design trade-offs among sensing margin, robustness, and low-power performance.

○ PLL DESIGN WITH 2.4/5 GHZ VCO

Mar 2026 – May 2026

- Working on a course project involving a PLL with a 2.4 GHz or 5 GHz VCO, a P/(P-1) dual-modulus divider, and 1 MHz frequency step.
- Reviewing the design of key building blocks, including the VCO, divider, phase detector, charge pump, and loop filter.
- Performing preliminary analysis, schematic design, and simulation for CMOS-based implementation.